REMARKS

Claims 1, 3, 5, 6, 8, 10, 15, 16, 18, 19, 20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54, 56-74, and 76-85 are pending in this case.

Claims 1, 3, 19, 20, 25, 38, 45, 48, 49, 52-54, 57, 60, 63, 66, 69, 71, 73, 76, 80 and 82 are amended herein.

No new Claims and no new matter have been added.

Claims 2, 4, 7, 9, 11-14, 17, 21, 27, 29, 35, 37, 39-44, 51, and 55 have previously been canceled in this case.

Double Patenting

The Examiner has provisionally rejected Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 23-26, 26, 30-34, 36, 38, 45, 46,48-50 and 56-61 as unpatentable on the ground nonstatutory obviousness-type double patenting as being unpatentable over claims 44-53 of copending U.S. Patent Application No. 08/483,938. Applicant has amended the claims to include: "A commercially mass-produced, integrated circuit (IC) having multiple active circuit components" and

"a solid state material region . . . together with said electronic rectifying barrier, electrically isolating a selected active circuit component from another neighboring active circuit component to make these two active circuit components electrically independently operable" to patentably differentiate from the claims of patent 7,038,290. This obviates the double patenting rejection.

Specification

The Examiner has objected to the specification, alleging that Claim 20 recites "a terminal portion" in line 17, but there is no antecedent basis for this term in the

specification. Applicant respectfully submits that this objection is obviated in view of the amendments to Claims 3 and 20.

Section 112, second paragraph, Rejections

The Examiner has rejected Claims 20, 22-26, 28, 30-34, 36, and 38 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In view of the amendments to these claims, Applicant respectfully submits that these rejections have been overcome.

Section 103 Rejections

The Examiner has rejected claims 1, 3, 5, 6, 8, 10, 18-20, 22-26, 28, 30-32, 34, 36, 38, 45, 46, 48-50, 56-58, 60, 63, 65, 67, 72, 73, 76, 77 and 85 under 35 U.S.C. §103 (a) as being unpatentable over U.S. Patent No. 4,916,716 to Fenner et al.("Fenner") in view of U.S. Patent No. 3,341,754 to Kellett et al ("Kellett"). These rejections are respectfully traversed.

Applicant notes that, as does the Examiner, Fenner does not disclose each and every limitation of the pending claims, as is required of a proper reference under Section 102. The Examiner states that the limitation at the end of Claim 1 would have been obvious, however, this cannot be the basis for the rejection under Section 102. Even if, arguendo, Fenner discloses the structural elements, the characteristic language noted by the Examiner cannot be ignored, as it necessarily further defines the structural elements of Applicant's invention. The Examiner is apparently attempting to argue that these properties are

inherent, but in fact they are an important aspect of Applicant's invention, and are not taught or disclosed by Fenner, and as such Fenner is not a proper reference under Section 102.

Applicant respectfully submits that for at least the following sixteen easons, the Fenner would not be a valid reference against the above 47 claims.

1) In the newly amended independent claims 1, 20, and 57, the new limitation of "a solid state material region ... and, together with electronic rectifying barrier, electrically isolating a selected active circuit said component (or transistors) from another neighboring active circuit component to make these two active circuit components electrically independently operable." --- the basic structure of **integrated circuits**. Fenner's device is **only one single unintegraed**, low-resistance mesa diode containing **only one** active circuit element, i.e., mesa diode. The simple diode has no other active circuit element to isolate from or to independently operate with;

2) All the three independent claims 1, 20, and 57 in this '081 case specifically claim "a commercially mass-produced integrated circuit" that calls for extremely high dimensional precision and quality/yield to be commercially profitable and mass-producible in the tough worldwide competition. Fenner, on the other hand, claims only a single, isolated unintegrated semiconductor diode device the yield and performance is not so critical. For example, a 10% yield on a

Fenner's devices gives 1,000 good diodes for sale in 10,000 produced. But on an integrated circuit device each containing only 1,000 or one million circuit components, the same 10% yield gives practically **zero** (i.e., 0.1 to the 1,000 or one million power) saleable products;

3) All the remaining independent claims require the isolating groove (solid state material region in claim 1, third solid state material body in claim 20, and device material region in claim 57, **directly** "contacting a non-vertical and expanded peripheral surface of the rectifying barrier". Fenner's channel 7 contacts the rectifying barrier 3/4 at a vertical and unexpanded peripheral surface of the rectifying barrier, directly opposite to what this invention specifically teaches and claims. Fenner's slanting or non-vertical passivating glass layer 6 (col. 3, lines 40-41) does not contact the vertically flat and unexpanded peripheral surface of the rectifying barrier 3/4, either. Li's earliest 3,430,109 of 1965 fully described the **detailed** procedure to design, make, use, and benefit from the new design. Fenner and Kellett neither disclosed, suggested, nor even hinted in their respective 1981 and 1966 patents. Anyway, Fenner is some 15 1/2 years later than Li's '109 patented invention filed in September 1965, even if Fenner enablingly disclosed;

4) The Fenner device also has only one single PN or Schottky **barrier**, and hermetically but only physically sealed, **not metallurgically bonded**, into a

"passivating" glass layer ('716, col. 2, line 44) or casing. This '081 invention is for **integrated circuits** containing **multiple**, up to millions or billions of, transistors on each chip with **vastly superior** cost, miniaturization, and performances;

5) With regard to Claims 1 and 23, Applicant respectfully submits that Fenner's device could not have "said solid state material region being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said rectifying barrier, without thermally and electrically insulating voids and micro cracks visible at 1,000 times magnification in interfacial bonding regions between the device components." One notes that Fenner's diodes contain many high-melting materials having melting points of over 1,000°C, and including GaAs ('716 at col. 2, line 47), W, Pt, Ti, Mo, and Ag ('716 at col. 2, lines 17) oxides and Cr ('716 at col. 2, line 68), ad Fe, Cu ('716 at col. 3, line 45) and glass. Vacuum deposition was at 90°C ('716 at col. 3, lines 20-21), while glass envelope fusion sealing at 600-650°C ('716 at col. 3, line 53). At these processing temperatures, except for the low-melting glass tube, there was **no** fusion, liquid diffusion, graded seal, and metallurgical bonding. Actually, bonding metals to nonmetallic such as GaAs, SiO2, and the always surface-oxidized metals to metals or other ceramics such as oxides, is a world-renowned, most difficult technology. Voids were unavoidable, particularly in packed solid particles from CVD and plating used by Fenner. Packing of even ideal,

spherical particles of equal size according to hexagonal or face-centered cubic structure produces at best only about 75% density, or with 25% of voids. These packed structures are, therefore, gas-permeable and non-passivating to the critical rectifying barrier. Fenner also used the classical chemical vapor deposition (CVD) methods producing up to 20% voids even in 1981. Electroplating also packs solid particles under voltage gradient to give tree-structures with never even close to 100% density. Porosity makes it difficult to modify and control the beneficial stresses and strains claimed in claims 25, 26, and 36;

6) Except for a few vertical thickness dimensions of the horizontal and flat or uncurved rectifying barrier thickness layers 3 and 4, Fenner disclosed no critical dimensions, materials, and interfacial qualities of the component materials disclosed or mentioned, such as thickness accurate to several hundred atomic layers, radius of curvature of "rounded" bottom of the **vertically uniformly flat** channel 7;

7) The Fenner patent had a filing date of February 12, 1981, some 18 ½ years later than the filing date of Li's patent No. 3,430,109 filed September 28, 1965. The '109 patent clearly discloses the use of **cylindrical** or other shaped isolating grooves of various bottom shapes (at col. 2, lines 4-6). The **curved bottom** of the isolating groove are **specially designed** not just to **directly** contact and guard the curved barrier peripheral surface, but more importantly: a) to **electrically passivate** the

rectifying barrier; b) to vertically **expand** the peripheral surface; c) to **reduce** the voltage gradient across the rectifying barrier; d) to **decrease** the leakage current; e) to **minimize** device breakdown failures; f) to electrically **isolate** an active circuit component from its neighboring active circuit elements on the same integrated circuit chip; and g) to **minimize** circuit element size achieving **maximal** device **speed and miniaturization** and making modern electronics possible. Fenner's invention can not have, and never suggested or hinted at, any one of these benefits. Nor can and did Kellett's;

8) In particular, the dimensions, accuracies, shapes, aspect ratios, and positions of Fenner's channel 7 is immaterial relative to Li's many benefits on device cost, speed, miniaturization, and other performances as claimed in this application. Claims 5, 6, 18, 20, 24, 45, 46, 24, 30, 48, 49, 50, 56, 57, 60, 63, 65, 67, and 73 are thus obviated;

9) Li's oxide groove has a cylindrically rounded bottom with zero bottom width and **directly contacting** the **curved** rectifying barrier to maximize device miniaturization for oxygen masked diffusion process, making modern microelectronics possible and helping everybody everywhere and everyday - - a great commercial success or even revolutionary breakthrough by solving the first worldwide leakage epidemic giving universally zero device yield. The bottom of the oxide groove is down to 0.1 or near zero microns below the PN junction region. As shown in '109 at col. 3, lines 65-

70, in microelectronics, a difference in vertical distance of mere 0.1, from 0 to 0.1 microns, can **infinitely** change the junction peripheral surface expansion, i.e., from infinity at zero microns (h = 0) to finite at h = 0.1 or 1 micron. Simultaneously, and device yield also increases **infinitely** from commercially viable to 0. These are **not** matters of change in degrees - - Hence, claim 85. Fenner has no such structures, particularly the oxide isolating groove with central or major-portion rounded bottom of zero width, and directly contacting a **matchingly rounded** and differentially expanded, peripheral surface of the barrier region positioned to achieve **proximate effects**. In fact, the seemingly rounded part of the Fenner's channel 7 is too low by at least 0.2 to 2 um ('716 at col. 2, lines 53-60). Even if the channel 7 has a "rounded" bottom, the bottom does not **directly** contact the rectifying barrier 3/4 at all, as required in **all** the newly amended independent claims;

Fenner could not even reliably and reproducibly mass-produce their mesa diodes because of the universal worldwide leakage epidemic at the time destroying most of the device yields. To achieve junction passivation, Li's oxide groove provides rounded PN junction peripheral surface with very large, surface or differential surface expansion for minimum field gradients and leakage currents but maximum breakdown voltages. Only automatic groove forming methods with real-time feed-back control, as disclosed in Li's '109 (at col. 2, lines 38-68) and other patents can reliably and reproducibly produce smaller than **submicron** groove

sizes, depths, and locations and, more importantly, any meaningful device yield to make the process commercially viable.

10) In Fenner's FIG. 1 singular diode device, the channel 7 does **not directly** contact a matchingly rounded and differentially expanded, peripheral surface of the barrier region sufficiently microscopically positioned to achieve improved "proximate effects" such as beneficial stresses and strains. Fenner invention was designed to achieve low-resistance mesa diode, certainly not to use stresses and strains to improve device performance. Li's invention requires the combination of groove bottom rounding, proximity to the rectifying barrier, non-porous materials, and perfect bonding between device components. These limitations would make claims 26 and 36 allowable;

11) Kellett makes semiconductor resistors by ion implantation. The lateral boundaries of the resistors are "relatively sharp ... with great accuracy down to some few hundred atomic layers" ('754, col. 3, lines 22-25). But there was no enabling disclosure of a method to make the implanted groove of a specific **shape** by a skilled person without undue experimentation. Nor do any one of the other ion implantation techniques cited in this '081 applications. Only Li clearly disclosed and described in detail an automatic mechanical grinding method with real-time feed-back control to achieve cylindrical, spherical, or conical grooves with **submicron dimensional and shape accuracies**, even in 1965. See Li's 109 patent at col.

2, lines 38-68;

12) In the Fenner Fig. 1 device, whether the 3/4 rectifying barrier between layers 3 and 4 is a PN junction or Schottky barrier, the **vertically flat or planar, non-curved, and unexpanded** (certainly not "differentially surface expanded") junction peripheral surface contacts the equally vertically flat or planar and having non-expanded nor differentially expanded side surface on the pocket 7;

13) Fenner's critical barrier-forming layer 3 is a weakly n-conductive semiconductor layer ('716 at col. 2, lines 58-59). The layer 3 thus still has orders of magnitude of free electronics and holes to carry electricity. It is still a semiconductor and functions not as an insulator or intrinsic semiconductor, but as a semiconductor with many, many free carriers therein to conduct electricity. Thus, the layer 3 is not an insulator at all, otherwise no PN junction or Schottky barrier, or semiconductor diode or transistor can ever form and there is no diode whatsoever. On the other hand, the intrinsic semiconductor is an insulator and stops electrical current dead cold. No PN junction, Schottky barrier, can form with an intrinsic semiconductor. Accordingly, the rejection of claim 22 would appear improper;

14) The n-conductive semiconductor layer 3 is also flat-sided and totally above the hemi cylindrically "rounded" channel bottom of channel 7. Hence, the PN or Schottky rectifying barrier 3/4 is already over 0.2

and 2 microns above the "curved" portion of the channel bottom 7. The rectifying barrier was physically guarded but not electrically passivated, and was easily contaminated by metals or dust particles to cause the same worldwide leakage current epidemic resulting in poor device yield and high cost, as explained in '109, at col. 4, line 56 to col. 5, line 41. Further, the flat-sided peripheral surface of the barrier has absolutely no surface expansion or differential surface expansion---another feature of the Li's unique oxide grooves. Accordingly, Fenner's device does not have passivated PN junctions, expanded barrier peripheral surface, and reduced voltage gradient thereacross, nor stress and strain relief for lack of curvature on the peripheral surface, and other features of Li's patented devices.

15) There is no other device to isolate from on the same chip. In the Fenner device, whether the annular channel 7 shape is cylindrical, spherical, paraboroidal, conical, flat, or rounded (See patent '109, col. 2, lines 5-6) had nothing to do with the device breakdown voltage, leakage current, and device yield, and little to do with the overall diode size or miniaturization. Yet device miniaturization is extremely important in modern microelectronics where high miniaturization is absolutely necessary. Without device yield, there was no products to sell. Without reduced device size, there is no device miniaturization and, therefore, modern electronics, regardless of what the channel 7 size, shape, thickness, or location. The dimension of the various diode dimensions, the accuracy

of the diode component dimensions, or the **bonding qualities** between the different diode component materials are then unimportant or irrelevant. As shown elsewhere, the rounded groove bottom with zero bottom width of Li's invention, alone, achieve junction passivation, reduced leakage current, increased breakdown voltage, improved device speed and other performances and, above all, make device miniaturization and modern electronics possible - - a great commercial success;

16) "Major-portion groove bottom rounding" is a key feature of Li's unique oxide-isolation grooves leading to high device yield and miniaturization. Many prior examiners have repeatedly rejected this feature under USC Section 103. These rejections were all overcome or reversed. In an Appeal on application Ser. No. 05/838,758 (patent No. 4,916,513), the Appeals Board on June 17, 1981 on page 5, lines 4-21 clearly stated that: "claims 2 through 5, 7, 8 and 10 through 19 all require that the depth of he groove vary along a major portion (more than half) of the groove width. Peltzer (3,648,125) does not **explicitly** disclose this feature. Nor is it apparent from the drawings that the curved portions at the bottom of the groove extend over more than half of the width of the groove. The examiner says that the appellant and Peltzer form their grooves in exactly the same manner; therefore, they must be identical. While Peltzer says that the grooves are etched in the epitaxial layer and then oxidized to form oxide isolation regions, no mention is made of the **cross-sectional shape** of the grooves. The appellant,

on the other hand, is **very concerned** about the cross-sectional shape of the groove. Therefore, we cannot say that the grooves of the appellant and Peltzer are formed in exactly the same manner. Therefore, we will not sustain the rejection of claims 2 through 5, 7, 8 and 10 through 19 under 35 U.S.C. 103 as anticipated by Peltzer."

In the same decision on page 6, lines 12-21, the Board says: "As for claims 2 through 5, 7, 8 and 10 through 19, Murphy (RE 2,653) clearly does **not disclose** a groove depth that varies along a major portion of the groove width, a requirement of all these claims. For the reasons we expressed before with respect to Peltzer, we cannot say that the appellant and Murphy form their grooves in the same manner. Finally, the examiner had not presented any other reason why this feature would have been obvious, and we know of none. Therefore, the rejection of claims 2 through 5, 7, 8 and 10 through 19 under 35 U.S.C. 103 as obvious in view of Murphy is reversed."

For many years after this decision, there were no more examiner's rejections of Li's groove having major-portion rounded groove bottom of zero width, based on nothing but draftsman's accidental disclosures of seemingly rounded groove bottoms.

Accordingly, without any specific teaching, one must consider Fenner's channel 7 rounding also as accidental disclosure. Fenner's short, 2 ½-page patent specification simply did not enablingly teach. Even if

Fenner invented this round-bottomed channel 7, it was in the wrong place, for the wrong purpose, and achieve totally different results. It was also some 17 ½ years later than Li's '109 invention. Hence, Applicant respectfully submits that all the rejections based on channel bottom rounding and vertical thickness change, such as on claims 1, 3, 5, 6, 8, 10, 26, 30, 31, 32, 34, 45, 46, 67, 73, 71, 73, 76, and 77 are thus obviated.

Applicant does not believe that Fenner has an enabling disclosure on the technologies of using unique materials thicknesses, configurations, and thermal mismatch coefficients, radii of curvature, processing steps, and equipment for making a commercially mass-producible and profitable integrated circuits according to the new technologies in Li's prior patents and applications.

Applicant respectfully submits that all the rejections have been obviated. As set forth in MPEP 706.02, in order to establish a prima facie case of obviousness, the Examiner must, among other things, provide an explanation as to why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed invention. In the present case, the Examiner states that such motivation would be due to "meet basic design needs". However, Applicant respectfully submits that this is not accurate.

Accordingly, withdrawal of the rejections under

Section 103 is appropriate and is respectfully requested.

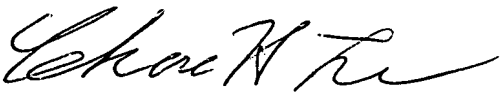
Claim 45 has been amended to limit said electronic rectifying barrier to be "differentially surface-expanded vertically" thereby obviating the rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and an early notice to that effect is respectfully requested.

Please direct any questions concerning this Response to Applicant's undersigned representative, who can be reached directly at (610) 869-6302.

Respectfully submitted,



Date: April 12, 2007

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Newly Cited References

The MPEP states that "for cases involving related patent invalidation and inequitable conduct," the Examiner must be clearly told and explained about the prior court decisions and other details. Accordingly, applicant hereby submit these "Other References" on a Toshiba-Li suit in which Toshiba Corporation falsely accused Li of "inequitable conduct" to the USPTO by failure to disclose a prior Appeals Board's adverse decision on a brother application Ser. No. 838,758 (838,758, U.S Pat. No. 4,916,513), thereby invalidating Li's 4,946,800 patent.

These references, already cited by the Examiner in Applicant's issued U.S. Patent No. 6,784,515 B1 as "Other Publications," are given below:

00-1451, Nov. 8, 2000, Federal Circuit Decision;
223-55, 1975, PTO Board Decisions; and
456-32, 1981 PTO Board Decisions.

In the 1996 Toshiba-Li case, Toshiba repeatedly and falsely accused Li for the knowingly false, non-disclosure of the "less than one micron" isolating oxide groove depth in the prosecution of the '800 patent. For example, "neither the parent '300 application, nor the grandparent '938 application disclose in any way that the groove depth is less than one micron," as unfortunately, **erroneously**, but **unintentionally** decided by the 1975 PTO Board Decisions.

In reality, the USPTO written records clearly shows that the short 5-page, double-spaced parent application No. 154,300 discloses 22 times the "less than one micron" groove feature, while the grandparent patent No. 3,585,714 (grandparent application No. 761,646) discloses the 1-micron feature at least **four** (4) times at: (a) groove depth "**h = 1 um** (micron = 10^{-4} cm)" at col. 5, line 69; (b) "local surface expansion is E_g = 70.7" at col. 5,

line 70; (c) "surface ... expansion ... of the junction region is 70.7" at col. 6, lines 42-45; and (d) "surface ... expanded 71 ... times" at col. 4, line 70. Through continuation-in-part (CIP) incorporation, the great grandparent patent No. 3,430,109 (great grandparent application No. 490,955) provides to the grandparent application No. 761,646 ('714 patent) four (4) more 1-micron (h = 1 micron) disclosures respectively at col./lines = 3/6-7, 3/69, 3/69-70, and 4/16-20.

The grandparent '714 patent (application 761,646) discloses the zero or near 0-microns feature (h = 0 um) at least **seven** times: (a) "**very** small values of h" at col. 5, line 66; (b) "with **very** small values of h, the local surface expansion E_g can even approach infinity" at col. 6, lines 35-36; (c) "maximum junction surface expansion with a cylindrical groove . . . the bottom terminal surface of the junction is tangential to the groove: at col. 6, lines 37-40; (d)"h = 0" at col. 6, line 43; (e)"junction region surface . . . selectively expand infinitely certain critical points or lines on the device" at col. 7, lines 12-15; (f) "For maximum surface expansion, . . . make h_m as close to zero as possible" at col. 8, line 61-62; and (g) "grooves are ... cylindrical and the bottom lines of the grooves just touch the lower end or terminal surface of the junction thereby achieving maximum surface expansion" at col. 9, lines 61-64. The great grandparent 490,955 application (patent 3,430,109) provides, through CIP continuity, to the grandparent 761,646 application ('714 patent) seven (7) more 0-micron (h = 0 micron) disclosures at col./lines = 3/68, 4/9-10, 4/12-15, 4/16-18, 4/59-61, 5/56-58, 6/20-22, respectively.

Each of the '714 and '109 patents additionally discloses both 50X and 500X groove surface expansions, respectively at col. 7, line 14 and col. 4, line 59. The 838,758 (Patent No. 4,916,513) Appeals Board's Decision dated August 12, 1981 on page 8, lines 21-25, page 2, lines 18-27, page 3, lines 13-16 stated: "this (30X surface expansion) in 154,300 application translates to a groove depth h (or h_m) of about

5 microns,.". Similarly, the 50X and 500X disclosures in the '714 ad '109 patents must translate to a distance of 2 and 0.1 microns. Also, disclosures of: "the . . . surface expansion . . . can easily exceed **30, 100**, or more times", on page 5, line 11 of the 154,300 application, must similarly translate into groove depths of 5 and 0.1 microns, respectively.

Altogether, the '714 and '109 patents clearly disclose **eight** (8) times the h = 1 microns, and **fourteen** (14) h = 0 microns, **twice** for both the h = 2 microns and h = 0.1 microns,

According to the 838,758 Appeals Board's decision on June 17, 1981 decision on page 8, line 21-25, the artisan would have it obvious to select the **eight** (8) 1.0 micron and the **fourteen** (14) zero microns to give **112** (8 x 14) more **0.1 micron** distances within the range (of 0 microns and 1 micron) specified. In addition, one can also combine the **two** 2-micron disclosures with the **fourteen** (14) zero-micron disclosure to provide **twenty-eight** (2 x 14) more 1.0 micron and **twenty-eight** (28) more 0.1 micron disclosures. The two 2-micron and the two 0.1-microns give four more 1-micron disclosures.

The total number of groove depth **disclosures** of "less than one micron" in the grandparent patent 3,585,714 is thus: **Fourty** (40 = 8 + 2 x 14 + 2 x 2) one micron, **142** (112 + 28 +2) 0.1 microns, and **fourteen** (14) zero microns, for a grand total of **196** (40 + 142 + 14) "less than one micron" depth disclosures in the grandparent 761,646 application.

The parent 154,300 application thus clearly discloses the 0 microns at the lowest point G **three times** on page 5, lines 7 and 5-7; page 8, lines 21-25; and in Fig. 1 at the lowest point G of the cylindrical groove bottom where the surface expansion is infinity. The '300 application further discloses each of the one micron and the two-micron depths **once** on page 8, line 22. In addition, the 154,300 application

also discloses, once each, for the 5 and 0.1 microns, as shown above. Using the same reasoning given above, the total number of "within one micron disclosures" in parent 154,300 application is **twenty-two** (**22**).

The grand total of "less than one-micron" groove depth **disclosures** in both the grandparent 761,646 and parent 154,300 applications is thus **two hundred and eighteen** (218 = 196 + 22), as shown in the Table on groove depth disclosures given below.

Table on Disclosures of Groove Depth Features

Application	h = 1.0	h = 0.1	h = 0 microns	Total
761,646	40	142	14	196
154,300	9	10	3	22
Total	49	152	17	**218**

Accordingly, the disclosure of the "within one micron" features must be **continuous and uninterrupted without any break** from the 490,955 of 1965 through the grandparent 761,646 and parent 154,300 to the 386,102 (patent 4,946,800 in suit) applications. This is so regardless of whether or not parent 154,300 incorporated the grandparent 761,646, or contains the Table 1 of the grandparent 761,646 application (Pat. No. 3,585,714) and, of course, whether the Table 1 in the grandparent 3,585,714 patent contains too few or too many expansion figures.

Hence, Toshiba **intentionally** and **100%** relying on the basic **false assumption** of "**nondisclosure**" of the within one-micron feature to "directly and convincingly **prove**" "Li's inequitable conduct." This "direct proof" caused the Judge to impose heavy financial penalties on the "injuring party Li" to the "injured party Toshiba."

Yet, the easily available USPTO **written records** clearly proves, for at

least **two hundred and eighteen (218)** times, that Toshiba was the real injuring party. Starting with the "non-disclosure" basic assumption, Toshiba further derived equally erroneous and unsupported opinions of "break in continuity", "later priority date", and "valid Peltzer, Sanders et al., and Li references". Further, Toshiba courageously presented all these false and false and misleading statements, **repeatedly**, to the Judge.

Hence, accusing Li even only **once** for "**non-disclosure**" of the groove depth in the grandparent 761,646 and parent 154,300 applications, Toshiba must have withheld **written** material information and abused the U.S. law **two hundred eighteen** (218) times, by misstating in court to the Judge that none of these **218** express depth disclosures ever existed. Toshiba's "**gigantic break** in Li's continuity of disclosure" of the groove depth feature thus becomes Toshiba's own "**gigantic misstatement or lie**". The other allegations were built on this false "non-disclosure" assumption and involved even more, some many more, law violations, due to various additional legal and technical reasons.

In my opinion, Toshiba misinformed, deceived the judge in court by making 11 false charges each repeated 1 to 115 times totaling some **52,570** law violations within some five short hours. **Solely orchestrating and 100% financing** the Toshiba-Li suit, the Toshiba **management** must be **fully responsible** for all these fictitious, fraudulent statements or representations. Of course, the Toshiba lawyers **knowingly, willfully, and deliberately** made all these false statements. But **Toshiba financially benefited 99.999 %** by willfully infringed the '800 patent annually many **trillion** times, i.e., millions of products such as memories each having millions or billions of memory cells with each cell containing 4 (top, right, bottom, and left) oxide isolating grooves that infringed all the 26 claims in the '800 patent.

Actually, a former technical, BS judge Cacheris already **meticulously** labored on this case for **months**, generated some **twenty carton boxes** of legally

reasoned documents, and decided correctly on 10 to 15 **technically complex** issues involved. Judge Cacheris's ruled all in favor of the Applicant, including:

1) On the groove depth feature **disclosure**, Judge Cacheris already decided that "it **need not be in writing**";

(2) Twice denied Toshiba's motion to change of venue;

(3) Ruled baseless a Toshiba's countersuit based on the RICO Act; and

(4) Denied Toshiba's motions in the Markman's hearing on the validity of the '800 claims.

Unfortunately, on the day of Jury selection, Judge Cacheris was sick and was replaced by a last-minute substitute, BA Judge Brinkema. Toshiba deceived this replacement judge into believing that the case involved only a "**simple procedural matter.**" Based only on some **274 pages** of court records, the new Judge summarily invalidated, within some **five fours**, Applicant's 4,946,800 patent.

On cross examination, Toshiba's own technical witness Harry Manbeck testified that "if the 0.1 microns is disclosed, it would flow through . . . change the whole matter", and "there would be **no break in continuity**", if there was (the 0.1 microns) disclosure **(A239 See Appeal No. 99-1451)**. As shown above, the 761,646 application contains for at least **142** times the 0.1 micron feature, while the 154,300 application discloses the 0.1 microns at least **ten** (10) times.

The 838,758 Appeals Bard **seriously erred**, **unintentionally**, by **wrongly** stating in their August 12, 1981 decision on page 3, lines 6-9 that: "Neither the parent (154,000) application nor the grandparent (761,646) application discloses **in any way** that the distance from the bottom of the groove to the PN junction should be less than one micron." Specifically, "the one-micron feature was both unsupported in the

reference table (Table 1) in the 761,646 application and not "included or specifically incorporated by reference in the 154,300 application. Hence the **chain of continuity** for this (within 1-micron) subject matter was **broken** by the parent application, Serial No. 154,300, and carried through to the parent application". See the Board's June 17, 1981 Board decision, page 4, lines 16-22.

Anyway, Toshiba never should have used the Pelzer, Murphy, and Sanders et al. as "**references**" against the claims in the '800 patent. The Sanders et al. V-groove reference was published in December 1973, even later than the '800 actual filing date. Nor did Sanders teach how to make his V-groove with an impossible **sharp notch**. Yet, Li actually invented the V-groove over in his '109 patent, and clearly disclosed in 1965 a way to make the V-groove with a conical grinding tool. See, Li's September 1965 greatgrand parent patent No. 3,430,109 at col. 2, line 6, over eight (8) years earlier than Sanders et al. IEEE paper published in December 1973.

Toshiba presented nothing at the Brinkema court except for unsupported assumptions, baseless hypotheses, ridiculous "Smoking guns", and knowingly false decisions by the 838,758 Appeals Board. But **solely coordinating, 100% financing, and 99.999% benefiting** all these illegal activities, the Toshiba management must be fully responsible for every knowingly false charge or illegal activity of their participating violators.

Accordingly, it was **not** Li, **not even once**, but Toshiba who committed, **tens of thousand times**, "**inequitable conduct**" against the U.S. Patent and Trademark Office, Patent system, and Judicial system. The '800 patent should **never** have been illegally confiscated. Certainly Toshiba must be the "injuring party", and I am the "injured party"; and not the other way around, as Toshiba proposed and Judge Brinkma accepted.

It was Toshiba who knowingly and persistently committed repeated inequitable conducts by purposely and selectively withholding critical

information, and making knowingly false statements. Toshiba falsely accused me on **349** false charges and seriously violated U.S. laws some **52,570** times in five short Brinkma Court hours averaging **10,514 times per hour**, a U.S. or even world record.

However, the 838,758 Appeals Board also made correct and important decisions, particularly as to the rounding feature of the oxide isolating groove bottoms. "Major-portion groove bottom rounding" is a key feature of Li's unique oxide-isolation grooves leading to high device yield and miniaturization. Many examiners have repeatedly rejected this feature under USC Section 103. These rejections were all overcome or reversed. The 05/838,758 (Li's patent No. 4,916,513) Appeals Board on June 17, 1981 on page 5, lines 4-21 clearly decided in favor of Li on this groove rounding issue, as shown above.

Hence, Examiner Saba, in his final Action allowing the '800 patent, stated that he allowed because of two limitations in all the claims: (a) major-portion groove bottom rounding; and (b) less than 0.1 micron groove depth disclosure. Toshiba never dealt the groove bottom rounding feature, consistently misstating that the less than one micron feature was never **disclosured** to the USPTO in connection with the '800 patent because Li, as Toshiba emphatically misstated in Court, **never** disclosed the "less than one micron" groove depth feature. In reality, this depth feature was disclosed 218 times, 196 times in the grandparent 761,646 application and 22 times in the parent 154,300 application.

The groove rounding allowed circuit miniaturization and modern IC. The importance of modern IC can be seen as follow. The Institute of Electrical and Electronics Engineers (IEEE) commemorated its 40th anniversary by asking 40 of the technology masterminds to vote on the most important technologies. The results are summarized in the November 2004 issue of the IEEE's Spectrum magazine at the tops of pages 38 and 39: "Take away the semiconductor, and all of electronics --- all of

it! --- collapses, along with all of the world's economies." That's how Nick Holonyak, Jr., University of Illinois professor, IEEE Medal of Honor winner, and inventor of the red light-emitting diode, views the incalculable contribution that the IC has made to society over the last four decades. According to Craig R. Barrett, CEO of Intel Corporation, the world's largest semiconductor manufacturer, the "most important technology of the last 40 years" is "the commercialization of the transistor. Without the invention of the integrated circuit (IC), the personal computer would have been the size of the Pentagon, and the cell phone the size of the Washington Monument. That is, the groove bottom rounding has been a great commercial success. Even Toshiba illegally made **billions** of dollars by willfully using this simple technique.

The oxide isolating grooves in the prior-art devices, such as those of Peltzer (Pat. No. 3,648,125) and Murphy (Pat. No. 3,649,386), all had large central flat bottoms wastefully occupying **major** portions of the chip real-estate. This waste of chip real-estate resulted in only a **minor** portion of the chip real-estate being used for the active transistors or diodes. These prior-art devices made device miniaturization impossible. Li's inventions overcome this serious problem.

A summary of Toshiba's Corporate Policy is given below.

Toshiba's Corporate Policy

The following incomplete news item s about the Toshiba Corporation mainly came from the Wall Street Journal 1987-1992, alone. These items prove that:

1. The intention of Japan as a whole and, in particular, of the Toshiba Corporation, is "to take over the World economy", according to the Wall Street Journal. See, Item D1 below. That is they want to conquer systematically the US and the entire World economically; after militarily failing to dominate US and the World even with the dirtiest Terrorist attack on Pearl Harbor and killing thousands of Americans in one morning, destroying most of our Pacific fleet, and slaughtering tens of thousands of American service men and tens of millions of innocent citizens in other countries.

2. Even the Japanese government finds out that "a system based on trust didn't work with the Toshiba Corporation". See Item A9.

3. Toshiba is the most law-violating company in Japan and US, France, and European community. See all items below. They violated US, Japan, and European laws on exporting, dumping (Items B1, B3, B5, B6, B10, C1, C3, and C6), price fixing, below-market pricing (Item C4), campaign contribution (Items B1, B5, B6, E6, and F6), customer duties laws (Item C2) . They even propped up domestic prices (Item F3), failed to fulfill signed agreements (Items A13,, B15, and F12), withheld advanced technology to US firms (Items E1 and E2), forbad retailers to advertise (Item F4), falsified invention record (H1), and violated the same laws after specifically ordered not to (Items A13 and B13, F1, and F2).

4. Toshiba's top executives including chairman, present, Chief Operating Officers, senior officers have been searched, arrested, banned, fined, sanctioned, forced to resign, and otherwise punished.

5. Toshiba's senior officers knew they were breaking the law while breaking the law (Item A13, B15, and F12). They were orders by their superiors to do the illegal acts.

6. Toshiba helps the then enemies Soviet Union and other enemies (Items A2-7, A13, B2, B4, , B7-8, b11-13) more than any other American or Japanese company, doing immeasurable damage to the US and Japan.

7. Refused to pay for willful patent infringements (Items E2, E3, E5, and G1).

8. US and Japanese courts severely punished Toshiba by heavy fines; bans, sanctions, and other severe punishments.

Hence, the Toshiba Corporation has a very long record of persistent, notorious corporation policy, behavior, and pattern to violate the US, Japanese, ad European laws. They repeatedly, deliberately, and knowingly misstated or simply lied in court (Item G1). From this extremely bad record, Toshiba does not have "clean hands" going to any U.S. court.

News Items by the Year

A. 1987

1. President Reagan imposed stiff tariffs of as much a 100% on products tailored to inflict severe penalties against six Japanese companies including Toshiba Corp. 4/20 3:1, also 3/27 3:1.

2. Japan police searched 13 offices and factories of Toshiba Machine Company units in connection to the units' alleged involvement in the illegal export of high-technology machine to the Soviet Union. 5/1 2:4.

3. Japan police arrested two executive of Toshiba Machine Company unit for their alleged role in the illegal export of high-technology machine tools to the Soviet Union 5/28 26:3.

4. Toshiba Corporation's Toshiba Machine Company Unit has contributed to the illegal export of sensitive technologies to the Soviet Union. 6/19 17:5.

5. Senate votes to bar Toshiba Corporation for US sale; sanction results from sale of militarily sensitive technology by the company to the Soviet. 7/1 4:1.

6. Toshiba's top two officers, chairman and present/CEO quit their posts; moves follow Senators' vote to punish Toshiba for sale of equipment to Soviet 7/2 3:1.

7. Toshiba's US customers say damage would be considerable for Toshiba itself, a target of congressional anger sparked by sales of militarily sensitive data to the Soviet Union 7/2 7:1.

8. Toshiba Basking: Members of the House, who laid out a Toshiba radio on the lawn of the Capital, and bashed it with a sledgehammer; action was allied to Senators' role to ban sales in the US of Toshiba products for at least two years. Case proves need for being more sensitive about defense. 7/2 18:1.

9. Japan's Ministry of International Trade and Industry, struggles to control Japan's exports; a system based on trust didn't work with the Toshiba Corporation. 7/13 9:1.

10. C. Itoh & Co. reacted strongly to reports it could be shut out of Pentagon contracts for its role in the Toshiba shipment 7/7 25:1

11. Commerce Department temporarily suspended the blanket authority of Japan's Toshiba Corporation to ship US products. 7/8 15:2.

12. The Pentagon has deferred doing any new business with the Toshiba Corporation. 8/19 14:4.

13. French government confirmed probe into Toshiba's illegal export; meanwhile, two senior Toshiba officers admitted in court they were aware that the sales were illegal. 9/11 23:2.

B. 1988

1. Consumer Department ruled that Japanese firms are selling 3 ½ inch computer microdisks to the US at low prices; preliminary finding and possibly stiff anti-dumping duties; probe was triggered by complaints lodge by Eastman Kodak's Verbatim corporation 9/27 - 54:5.

2. Japan's Ministry of International Trade and Industry announced April 28 that a Japanese shipment of 500 personal computers and discovered they were bound for North Korea; disclosure comes amid continuing anger in US over Toshiba Corporation 1987 shipment of high-technology equipment to the Soviet Union 4/29 - 20:3.

3. The Commerce Market imposed anti-dumping duties on 15 Japanese makers of computers and printers. 5/27 14:2.

4. The Pentagon, carrying out a law suspending Toshiba Corporation of Japan from defense business for six months, as punished for export control violations committed by their units 2/12 23:3.

5. Europe Community Commission started an anti-dumping investigation of several Japanese photocopier manufacturers including Toshiba Corporation. 2/18 14:4.

6. European Community Commission proposed levying dumping duties for Japanese firms including Toshiba Corporation. 3/8 31:4.

7. Tokyo District Court fined Toshiba's machine Unit two million yens for illegally selling sophisticated technology to the Soviet Union and gave suspended sanctions to two former executive of the unit. 3/23 22:2.

8. Japanese government, taking tough stance toward export violations, charged two Tokyo companies including Toshiba corporation, with illegally shipping electronic measuring equipment to China; action came at sensitive time as US considers Toshiba sanctions 4/6 20:1.

9. The Reagan administration is upset about provisions of trade bill that would ban further violation of export controls for selling to US, or contracting with US government for two years, bills encountered little opposition because of attention on sections dealing with retroactive punishment of Toshiba Corp. 4/15 20:1.

10. European Commission (EC) for the first time imposed anti-dumping duties on Japanese products manufacturers within the EC, move affects five European units of five companies including Toshiba Corporation. 4/20 18:4.

11. France arrested four current and former executives for the illicit export of technologies to Soviet Union; new scandal also involves a company also connected to the Toshiba scandal. 4/25 23:2.

12. Japan's Ministry of International Trade and Industry announced April 28 that NEC cancelled orders for products bound for North Korea, amid continuing anger in US over Toshiba units' 1987 shipment of high-technology equipment to the Soviet Union 4/29 20:3.

13. Toshiba Machine Company eventually will have to reduce its US operations because of a forthcoming three-year ban on its exports to the US; sanctions which apply also to parent Toshiba Corporation, are in reaction to Toshiba Machines' illicit sale to the Soviet of certain military equipment. 8/12-10:4.

14. Toshiba Basing: members of the House, who laid out a Toshiba radio on the lawn of the Capital, and bashed it with a sledgehammer; action was alleged to Senators' role to ban sales in the US of Toshiba products for at least two years. Case proves need for the need for being more sensitive about defense. 7/2 18:1.

15. US Senator Jake Garn charged that Toshiba Machine Company unit is trying to send its products to US buyers before a three-year ban on such sales can be enforced. 1/6 B8:6.

C. 1989

1. Commerce Department confirmed a preliminary finding that Japanese-made computer microdisks are being "dumped" into US. 2/8 - B3:5.

2. The US is investigating whether Japanese companies cheated it out of custom duties. 30 agents raided the firms 6/5 - A7:2.

3. The Commerce Department, upholding trade complaints filed by AT&T issued preliminary rulings that manufactures of business telephone system in Japan (Toshiba) for dumping in the US. 7/28 - A2:4.

4. The Commerce Department confirmed its earlier finding that Toshiba Corporation sold at below market prices in the US 10/12 - B11:3.

5. The Justice Department ended its previous announced investigation of Toshiba Corporation's $167 million requisition. 11/17 - B5:4.

6. International Trade Commission cleared the way for the imposition of anti-dumping duties on more than $1 billion a year in imports of small business-telephone systems from Toshiba Corporation and other companies, in a major victory for AT&T. 11/ 21 - A5:1.

D. 1990

1. A proposed Japanese Consortium aimed at developing a world-wide standard for future factory technologies and to pool international resources has triggered protests in U.S. and Europe, where some officials claim the Japanese intension is to take over the world economy (L) 5/1 - A15:2.

E. 1991

1. A commerce Department reports says there is "evidence that certain Japanese companies have injured U.S. semiconductor chip makers by withholding state-of-the-art processing equipment from them while providing the same technology to Japanese manufacturers (M) 5/6 -B4:3.

2. Sen. Lloyd Bentsen and Sematch, a U.S. company, released lists of Japanese companies they said purposely withheld advanced manufacturing equipment form U.S. chip makers with the aim of keeping Japanese companies dominant. (M) 5/7 -A16:1.

3. The brewing legal clash between Texas Instrument Inc. transcends the millions of dollars in royalty payments at stack in a classic bilateral battle of technological pride. The U.S. claims Japanese prowess, but the Japanese refutes the claim (L) 7/22 - A6:4.

4. A US district court in Alexandria Virginia banned Toshiba Corporation. For US manufacture or sale of single in-line memory modules, known as SIMMS, a package of memory chips that is used by most makers of personal computers (pc) compatible with IBM PCs. (M) 10/11 - B4:1.

5. Wang Laboratories Inc. said it won a lawsuit against Toshiba Corporation that could result in patent royalties of $8-12 millions a year (M) 8/16 - B3:1.

F. 1992

1. The Semiconductor Industry Association will seek trade sanctions of Japan does not fulfill its commitment under a 1991 agreement to increase foreign company's share of its huge chip market. Group members having been growing increasingly impatient with Japan (M) 3/12 - B3:4

2. After a two-month interagency study found that Japan has made insufficient progress in opening its markets to foreign semiconductor products. US Trade representative Carla Hills warned that the US would take "additional actions, as necessary". Under an August 1991 semiconductor accord, Japan accepted the goal of boasting foreign market share to 20% by the end 1992 but it has remained flat at 14.6% (M) 8/5, - B2:3.

3. Japan's Fair Trade Commission is investigating whether four leading electronic companies including Toshiba Corporation have been illegally propping up domestic prices of TV sets, portable video cameras, and other popular home electronics products (M) 3/27 - A3:2.

4. Japan's Fair Trade Commission is investigating whether four companies including Toshiba Corporation illegally forbade retailers to advertise retail prices on TVs and other consumer electronics items below certain levels (M) 3/26 - A10:4.

5. Two Japanese papers have reported that a unit of Loral Corporation has sued about 30 electrical appliance makers, mostly Japanese, alleging patent infringement. The suit seeks several billions in damages from firms including Toshiba Corporation (S) 3/26 - A16:2.

6. Toshiba Corporation's US subsidiary, Toshiba America Inc, its executives at the Tennessee Consumer Products division and its industrial electronics division in California agree to pay more than $18,000 in fines to FEC for making illegal contributions to several 1988 federal campaigns hidden under name of two top executives (M) 7/1 - A10:1.

G 1998-2003

Li invented **low-cost, highly** miniaturized integrated circuits (Patent 4,946,800) to overcome in the later 1950's the worldwide epidemic problems of poor **device yield, performance, miniaturization, and cost**. Li therefore collected royalties on his patent from a dozen of the world's large, resourceful, and **honest** companies who benefited from the '800 patent.. Toshiba befitted greatly by the invention and **willfully** infringed the patent many **trillion** times each year, but refused to get a license, even though they were warned by their own financial consultant for the high risks. They still counter sued accusing Li for "**extorting huge taxes** on the entire semiconductor industry", insulting the U.S. patent, the inventor, the already-licensed honest companies, and the U.S. patent and judicial systems. They employed dozens of top law firms in major U.S. cities, and withheld material information, misstated, lied, or perjured in court to the judge about the "non-disclosure" of claimed feature. In fact, the specifications expressly disclosed the feature over **107** times in **the few hours** of the court time. Toshiba simply misstated to the non-technical judge that none of each of 107 disclosures ever existed. The only single charge was "non-disclosure" of a claimed device dimension leading to "inequitable conduct". But a former BS judge already decided clearly: "**No need** for additional written disclosure" and Toshiba's own technical witness testified that "there was **no** break" in disclosure continuity. Further, the USPTO **written records** show **107** of the such required disclosures. Any one of these disclosures would disprove Toshiba's false charge. The U.S. Supreme Court noted that "there is no finding that Li had such knowledge", "the dispositve factual issue was whether Li knew ... There is no express finding to this effect". The Supreme Court also did not like the Toshiba's arguments, nor the conduct of the District Court and the federal Appeals Court in this case. Nonetheless, the Toshiba's **multiple** teams of lawyers in **many** top U.S. cities deceived the non-technical, unprepared and impatient judge, who summarily declared Toshiba as the "**injured party**", while Li the "**injuring party** and an "**inequitable conductor**" . The judge further invalidated the '800 patent, and imposed heavy fines on the inventor. This suit was a great insult to the inventor, the US patent, and the US patent and judicial systems, not to say instantly causing the **Nation trillion** to lose billions or trillion dollar at a time of major trade deficits.

Using the same dozen of U.S. law firms and the U.S. Courts, Toshiba is suing for patent infringement, and not extorting "huge taxes" as Toshiba called Li's patent licensing, asking for **hundreds of million dollars** at royalty rates orders of magnitude higher than Li was asking. Why should any inventors be so advantaged, even in the U.S. court, relative to a well-known, **notorious** world-infamous law-breaking company?

H. 2002

Toshiba's top research personnel swindled the IEEE Society to ask them to deliver the first, and most-prestigious, conference-opening **review paper** on their newly "**invented**" "single-electron devices" at the 2002 IEEE Electron Device Conference in California. But the Toshiba "invention", if any ever existed,

actually was exclusively on "plural electron devices," not "**single electron devices**" at all. Li pointed out at the Conference that they were mixing up "**single electron devices**" with **"plural electron devices**. Their top research personnel thereby joined their chairmen, presidents, and senior officers in knowingly and repeatedly **misstating or lying** in a most esteemed, conference in the world, damaging the IEEE Society and insulting thousands of busy Conference attendees who expected to learn about great new inventions in such a premier Conference. More alarmingly, Toshiba may use their ill-gotten "patents" to **"earn" billions** of dollars in annual sales and to extort, in U.S. courts, hundreds of millions or billions of dollars in taxes on U.S. companies, based on their illegal patents on something they never invented. The USPTO examiners never could have the resources to deal with Toshiba's innumerable savvy but egregious legal teams. How could USPTO prepare to prevent possible dishonest inventors? Even the Japanese government finds out that "a system based on **trust** didn't work with the Toshiba Corporation." See Item A9 above.